IN THE SPECIFICATION:

Amend the specification as shown:

[0037] Figure 1 illustrates a portion of a silicon wafer 10 after a number of preliminary steps including forming pad oxide 20, pad nitride 30, forming a deep trench (nominally about 8 microns deep and having an aspect ratio of greater than 40) in a conventional reactive ion etch step, filling the trench with a temporary filler material 110, illustratively spin-on glass (SOG) and recessing the SOG to provide room for forming a dielectric collar. A conventional planarizing step, e.g. by chemical-mechanical polishing, may be performed at any convenient time.

[0042] After the spacer material has been put down and the material on the bottom of the aperture 150 has been etched to form the spacer itself, the SOG material is removed, e.g. in a wet etch process, as shown in fig 3, leaving the entire depth of the trench, shown as aperture 155, ready for doping the buried plate 40, e.g. by gas phase doping shown in Fig. 4 with capacitor dielectric 45 and buried plate 40. Further steps of depositing the node dielectric and filling the trench with the center electrode to complete the capacitor.

[0043] In another aspect of the invention, a conventional process of depositing low pressure nitride may be used for the spacers, as shown in Figure 5. In that case, the SOG is a thermally stable material, e.g. polysilazane, that is cured at a temperature of less than 450C and then annealed, either in an oxygen ambient or in an ambient containing water vapor, at a relatively high temperature of 700 - 1200 C. Inert ambient anneal typically produces high tensile stress in SOG and could cause cracking. With annealing, the SOG can withstand the deposition temperature of LP nitride (600-800C), which provides a considerable advantage and process simplification over the prior art of a resist fill. ~~The~~ Figure 4 shows the result after stripping the temporary filler material, leaving the aperture 160 (in this case having been extended in a bottle etch step), with a capacitor dielectric 45 and ~~sidewalls 125~~ spacers 120 This step of performing the bottle etch precedes the step of depositing a thermally stable filler material.

[0045] Figure 6A shows an overall view of a trench after a "bottle etch" step of widening the aperture that will hold the capacitor and showing in detail 5 the location of a possible parasitic FET. In Figure 6B, dotted oval 130 ~~encloses~~ denotes schematically the vertical cell transistor, with gate 135, gate dielectric 133, body 134, and lower electrode/buried strap 132. The dotted oval 127 encloses an area extending from the buried plate 40 of the capacitor to the buried strap 132 of the vertical transistor 130. When the voltage on the center electrode 165 of the capacitor is high, there is a potential for the formation of a parasitic transistor, with electrode 165 as

the gate, collar 125 as the gate dielectric, buried plate 40 as one electrode and buried strap 132 as the other electrode.